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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/707,396 | 12/10/2003 | Ching-Nan Hsiao | NTCP0020USA | 1395 |

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(NAIPC) NORTH AMERICA INTERNATIONAL PATENT OFFICE
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| EXAMINER |
|---|
| GEBREMARIAM, SAMUEL A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/707,396 | HSIAO ET AL. | |
| | Examiner | Art Unit | |
| | Samuel A. Gebremariam | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman et al. US patent No. 6,605,838, in view of Nitayama et al. US patent No. 6,236,079.

Regarding claim 1, Mandelman teaches (fig. 2) a vertical dynamic random access memory (DRAM) comprising: a substrate (50) comprising at least a deep trench (56) having an upper trench portion (region where element 80 is formed) and a lower trench portion (region where element 70 is formed); a trench capacitor (70) located in the lower trench portion; a source-isolation oxide layer (88, referred here trench top oxide) located on the trench capacitor (70); and a vertical transistor (80) located on the source-isolation oxide layer (88), the vertical transistor comprising: an annular source (86) set in the substrate next to the source-isolation oxide layer (88), the annular source being electrically connected to the trench capacitor (fig. 2); a gate conductive layer (84) filling the upper trench portion; a cylindrical gate dielectric layer (82) located on a surface of a sidewall of the upper trench portion and circularly encompassing the gate conductive layer; and an annular drain (52) circularly encompassing the deep trench near a surface of the substrate (50).

Mandelman does not explicitly teach that a shallow trench isolation (STI) positioned around the deep trench; the gate conductive layer is electrically connected to a first contact plug and the annular drain being electrically connected to a second contact plug and the annular trench positioned next to the STI and the annular drains of adjacent vertical transistors isolated from each other by the STI.

It is conventional and also taught by Nitayama (figs. 4A and 4B) forming contact structure (112) on a gate conductive layer (124) and also making contact structure (106) on a drain region (134) in order to make contact to other portion of an integrated circuit device. Nitayama also teaches (fig. 4B) the use of STI structures (108) positioned around deep trenches (110).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the gate and drain contact in the structure taught by Nitayama in the structure of Mandelman in order to make contact to other portion of the integrated circuit. Furthermore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the STI structures taught by Nitayama in the structure of Mandelman in order to provide better isolation. The modified structure of Mandelman and Nitayama would have an STI around the deep trench and annular drains of adjacent vertical transistors isolated from each other by the STI.

Regarding claim 2, Mandelman teaches substantially the entire claimed structure of claim 1 above including a storage node filling (68) the lower trench portion and electrically connected to the annular source (86); a capacitor dielectric layer (66)

encompassing the storage node; and a buried plate (64) located in the substrate in a side of the capacitor dielectric layer.

Regarding claim 3, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the buried plate (64) surrounds a sidewall of the lower trench portion, and the capacitor dielectric layer (66) is located on a surface of the sidewall of the lower trench portion so as to isolate the storage node and the buried plate.

Regarding 4, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the trench capacitor further comprises a buried strap (86) for electrically connecting the annular source and the storage node (col. 5, lines 10-20).

Regarding claim 5, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the buried strap (86, col. 5, lines 10-20) is an annular conductive strap located on the surface of the sidewall of the lower trench portion above the capacitor dielectric layer (66).

Regarding claim 6, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including a conductive layer (103, fig. 4A) located on the gate conductive layer for electrically connecting the gate conductive layer and the first contact plug.

The combined structure of Mandelman and Nitayama provides conductive layer located on the gate conductive layer for electrically connecting the gate conductive layer (metallization layers or metal lines) and the first contact plug.

Regarding claim 7, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the annular source is an ion diffusion area (col. 5, lines 10-20).

Regarding claim 8, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the annular drain is a heavily doped area.

The limitation that annular drain overlaps ion implantation area is not given patentable weight, because it is product by process claim. "[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 9, Mandelman teaches substantially the entire claimed structure of claim 1 above including a passivation layer (152, Nitayama) covering the surface of the substrate and the transistor.

Regarding claim 10, Mandelman teaches (fig. 2) substantially the entire claimed structure of claim 1 above including the first and the second contact plug are electrically connected to a word line and a bit line respectively (col. 9, lines 1-5, Mandelman).

Regarding claim 11, Mandelman teaches substantially the entire claimed structure of claim 1 above the STI surrounds the annular source and the annular drain region without overlapping the deep trench (fig. 4B of Nitayama).

Regarding claim 12, Mandelman teaches substantially the entire claimed structure of claim 1 above including an annular spacer (140) surrounding the upper portion (refer to fig. 4A).

Regarding claim 13, Mandelman teaches substantially the entire claimed structure of claim 1 above including the second contact plug (106) has an asymmetric structure (refer to fig. 4A), which is positioned on the spacer (140) and the drain (134) while contacts the spacer (140) and the drain (134) at the same time.

***Response to Arguments***

3. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
August 22, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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